Through-silicon via based 3D IC technology: Electrostatic simulations for design methodology

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Abstract

Two parallel methods of simulation have been developed in order to evaluate the electrostatic impact that a through-silicon via (TSV) may have on a 65 nm MOS transistor. The first model is based on the finite element method (FEM) and the second one is related to electric component models (SPICE language). Both approaches are then compared and discussed. The SPICE model has been calibrated on the numerical one, so that it can be used for more complex devices – here, an inverter – and more systematic investigations. A range of 3D-compatible design rules have been defined. By integrating these new data on a complete 3D design methodology, we are able to design and layout simple logic circuitries based on a 2-stratum 3D architecture.

Introduction

As 2-dimensional IC scaling becomes more and more difficult to achieve for the next technological nodes, 3D IC technology is being considered as a real breakthrough approach. It seems to be an interesting solution in terms of IC design and manufacturing [1,2]. 3D integration doubtlessly brings significant benefits concerning circuit performance, density of integration, interconnect power consumption and heterogeneous technology integration capabilities [3]. Microelectronics worldwide actors tend to develop a through-silicon via technology (TSV) in order to connect stacked ICs to each others. TSV appears to be one of the greatest technology challenges brought by 3D integration. As TSV can be considered as a brand new entity in conventional IC architectures, electrical parasitic coupling and critical substrate noise might occur in neighboring active devices. These electrostatic phenomena have to be taken into account to ensure reliable circuit design [4]. Quantifying such effects allows designers to fit 2D design rules to 3D requirements. Another serious issue about 3D technology is that current design tools do not include 3D layout possibilities yet. Beyond TSV considerations, all the conventional design procedures and layout capabilities are unsuitable for 3D integration. At that time, only few labs or companies had developed 3D-compatible design methodologies that could lead to an electrical demonstration [2,5,6,7], but they are not commercially available. Allowing 3D design for the current 2D tools will fully release all the powerful capabilities of vertical architecture.

Copper TSV based 3D integration

There are many possibilities to integrate vertically two (or more) active strata, depending on the application-driven choice and the available 3D process steps. Bonding techniques (molecular, BCB, metal, etc), upper wafer orientations (face-to-face or back-to-face), remaining silicon thickness, alignment techniques are as many parameters that will impact design.

In this paper, we focus on a two-stratum integration flow developed at the CEA/Léti, using molecular bonding [8,9] that can be achieved either by wafer-to-wafer or die-to-wafer techniques. The two active bulk strata are face-to-face oriented. Top stratum backside silicon is thinned down to about 10 µm. Two kinds of through-silicon vias are integrated: one to connect the top metal layer to the metal 1 of top stratum, and another one to connect the top metal layer to the last metal level of bottom stratum (Figure 1). TSV are etched, isolated with oxide and filled with copper. TSV dimensions are typically 2-3 µm wide and 10-12 µm deep. The top metal layer is then deposited over the backside thin silicon layer in order to interconnect TSV to each other. Top metal layer dimensions are relaxed compared to the other metal lines because I/Os are also designed at the same physical level. I/Os involve wide metal lines to enable distribution of power, clock signals and ESD protections.

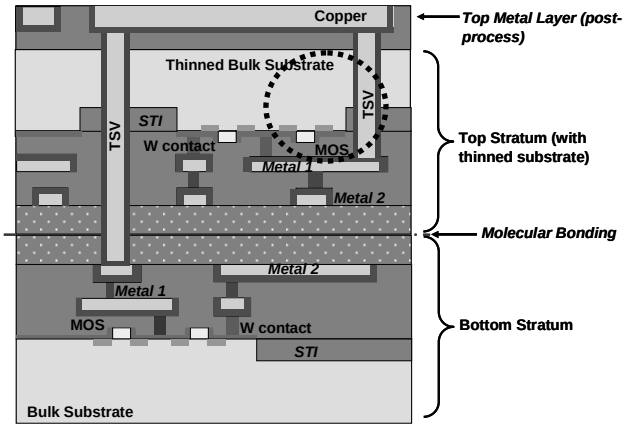

Figure 1. Copper TSV-based bulk face-to-face integration, using molecular bonding.

2D FEM modeling of TSV-induced electrostatic impact on device performances

In all 3D integration schemes, only the top stratum is clearly exposed to the electrostatic disturbances that may be produced by TSV. Indeed, bottom stratum devices are protected by the fact that TSV are connected to the last metal level of the interconnect network, far from the active area. Top stratum devices could be surrounded by several TSV that all pass through the thinned silicon substrate. This study is focused on TSV-CMOS local area depicted on Figure 1 (dotted line), and works with any 3D integration scheme.

In order to quantify parasitic coupling within the thinned silicon substrate, a simple structure is numerically meshed, using the finite elements method. The 2D TCAD software used is Silvaco Atlas [10]. A single 65 nm-based, low power MOS transistor implemented in the thinned silicon substrate and located near a TSV is considered. The whole structure is depicted on Figure 2 – left (dimensions are not scaled). The electrical behavior of the MOS transistor is simulated by the SIMS-based doping profile of 65 nm CMOS technology. As TSV dimensions are much bigger than the MOS ones, meshing the entire TSV is difficult because of the limited number of meshing nodes. So, TSV is considered as a perfect conductor and is represented on the structure as an electrode applied on the whole left vertical limit of the meshing.
To validate the FEM-based model, MOS electrical behavior has been calibrated on the 65 nm electrical models (Design Kit). It is shown that the (I_{on}/I_{off}) ratio from TCAD is 1.2 time higher than the one from the design kit model. TCAD-based threshold voltage V_T is equal to 0.41 V, *i.e.* 0.1 V lower than the design kit-based V_T. The MOS electrical behavior obtained by FEM-based simulation is very close to its design kit-based model.

The MOS transistor is plugged on its static mode (Vg = Vd = 1.2 V). A square voltage V_{TSV} (f = 200 MHz, 200 ps-long rising and falling ramp times, 3.3 V peak voltage) is then applied on the TSV. A local body potential V_B, located in between the channel at 0.5 µm under the oxide-silicon interface, is extracted during a transient analysis. This position enables to quantify the finest electrical disturbances that may modify the electrical behavior of carriers in the channel. We observed that body potential peaks occur at each rising and falling V_{TSV} ramp (Figure 2 – right). Distances between body contact and TSV (D_{via}), body contact and MOS (D_{body}) and substrate thickness (T_{sub}) were parameterized to evaluate the direct influence of the structure geometry on substrate noise. Maximal values of V_B were extracted when decreasing D_{via} value and increasing D_{body} and T_{sub} values (as shown on Figure 3). From that, T_{sub} is set to 10µm, which is a feasible technological requirement.

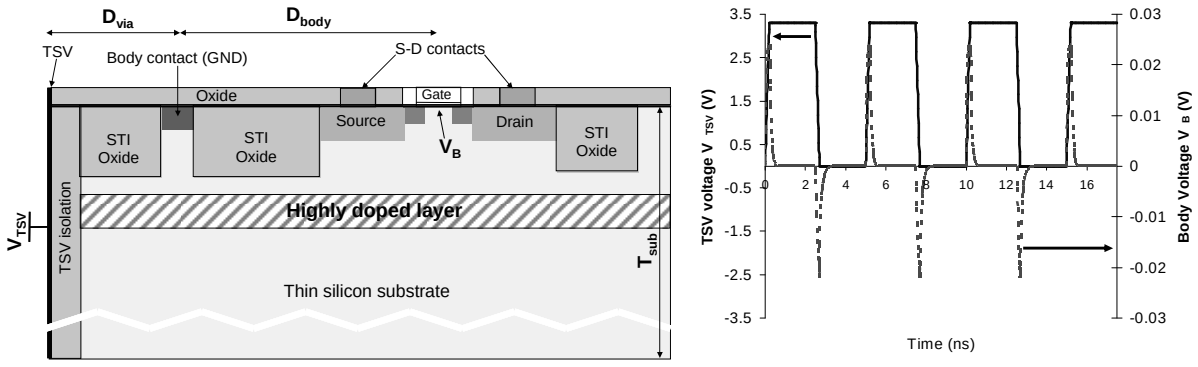

Figure 2. (Left) Structure for 2D TCAD simulations (not at scale) - (Right) Transient analysis of V_B and V_{TSV}

2D SPICE modeling of CMOS devices within a 3D integration

The previous numerical simulation allows the extraction of physics-based results. Nevertheless, the cost of simulation time is expensive. One solution is to employ SPICE-like simulation using a circuit simulator (Eldo) in which the results are quasi instantaneous. For this reason, the previous structure was adapted to simulate the impact of the TSV with circuit simulator. The silicon substrate model is composed of 3400 resistors approximately with a grid defined by $\Delta x=0.5\mu m$ (horizontal) and $\Delta y=T_{Sub}/20$ (vertical). The barrier oxide is modeled by a set of MOS capacitances. Finally, the MOS transistor is modeled using BSIM4.
To compare numerical simulation with circuit simulation, a set of numerical simulations was performed using a n-channel transistor with channel length and width L=W=1µm. The substrate thickness value is 10µm.
Figure 3 compares both approaches where the peak of body voltage (from Figure 2 - right) is plotted as a function of body contact-to-transistor distance (D_{body}) and TSV-to-body contact distance (D_{via}). Note that substrate and highly doped layer resistivities are adjusted for SPICE simulation to fit perfectly with the numerical simulations.

These last figures validate the SPICE-like approach for a wide range of distances. In the next part, this approach will be used to estimate the influence of the TSV on circuit performances for digital and analog applications.

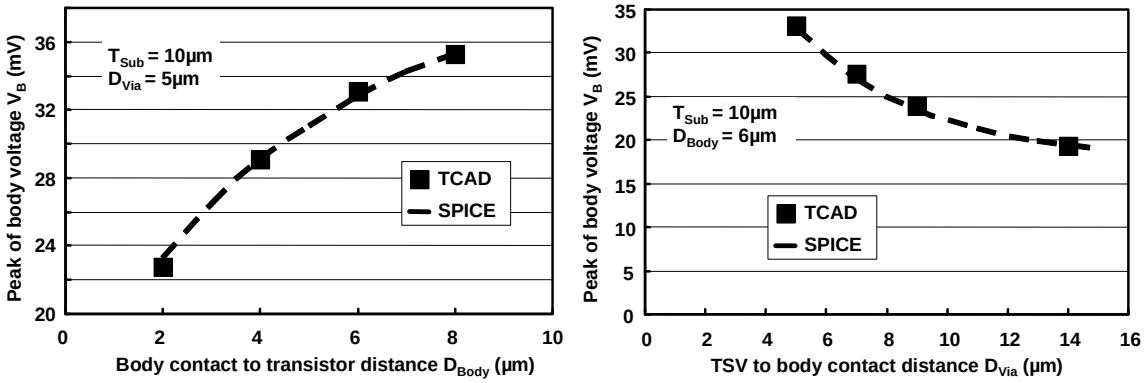

Figure 3. Comparison between TCAD and SPICE simulations: peak of body voltage V_B versus body contact-to-transistor distance D_{Body} (Left) and versus TSV-to-body contact distance D_{Via} (Right).

Estimation of the impact of TSV on circuit performances

The aim of this section is to evaluate the impact of the TSV on the circuit operations. To achieve it, basic simulations were performed using the SPICE-based model. On one hand, we propose to study TSV impact on the inverter in transient simulation for digital applications. On the other hand, the impact of coupling between the TSV and the transistor in AC and noise simulations is investigated for analog applications. These textbook cases could be used to define new design rules to preserve circuit performances.

Digital applications

This part is based on the investigation of inverter behavior in transient simulation. This inverter is designed with a 2D approach, as illustrated on Figure 4. pMOSFET is realized in n-doped region. Compared to nMOSFET, the p-channel transistor is less sensitive to fluctuations of substrate potential. In order to simplify the study, a coupling only between the TSV and the nMOSFET body voltage is supposed.
Device geometries are W/L=120nm/65nm and W/L=240nm/65nm for n and pMOSFET, respectively. Square signals are applied on the TSV, noted V_{TSV}, and on the input of inverter, noted V_{IN}, at 200MHz and 72MHz frequencies respectively. A capacitance load of 200 fF is plugged at the inverter output.

Figure 5 shows the results of the transient simulation on two configurations D_{Via}=1µm and 9µm. Spikes on the nMOS body voltage appear during the rising and falling ramp times of TSV and input voltages. Nevertheless, the output voltage is not affected by the commutation of TSV voltage. The output voltage dispersion due to the TSV switching is estimated lower than 500 µV for the worst case. From these results, it seems that the TSV has quite no influence on digital circuit behavior. In addition, these results obtained using a 2D approach are probably pessimistic compared to a 3D simulation where body control with the body contacts will be more efficient. As a conclusion, specific design rules are not necessary for this type of application. Design rules will be only defined from technological and process points of view (mask alignment for example).

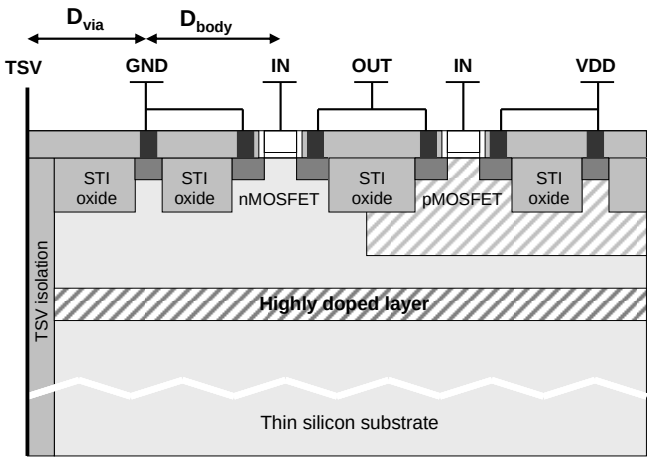

Figure 4. Schematic cross section of inverter.

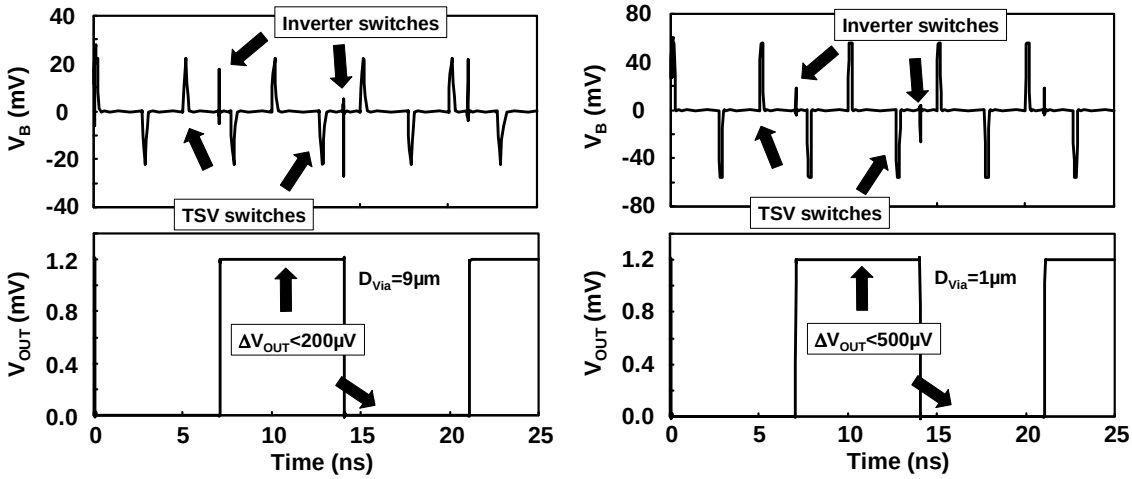

Figure 5. Transient simulation of inverter with D_{Body}=5.0µm and (Left) D_{Via}=9µm and (Right) D_{Via}=1µm.

Analog applications

The aim of this paragraph is to highlight the parasitic coupling between the transistor and the TSV.

A small signal voltage source dV_{TSV} is applied on the TSV. The isolation dV_B/dV_{TSV} is calculated from AC simulation. The transistor is a nMOSFET with L=65nm and W=1µm. This coupling is a high-pass filter due to the TSV insulator as shown on Figure 6 (Left) where dV_B/dV_{TSV}, noted H, is calculated versus frequency. On this figure, H_{min} is the minimum of the isolation and f_C is its cut-off frequency.

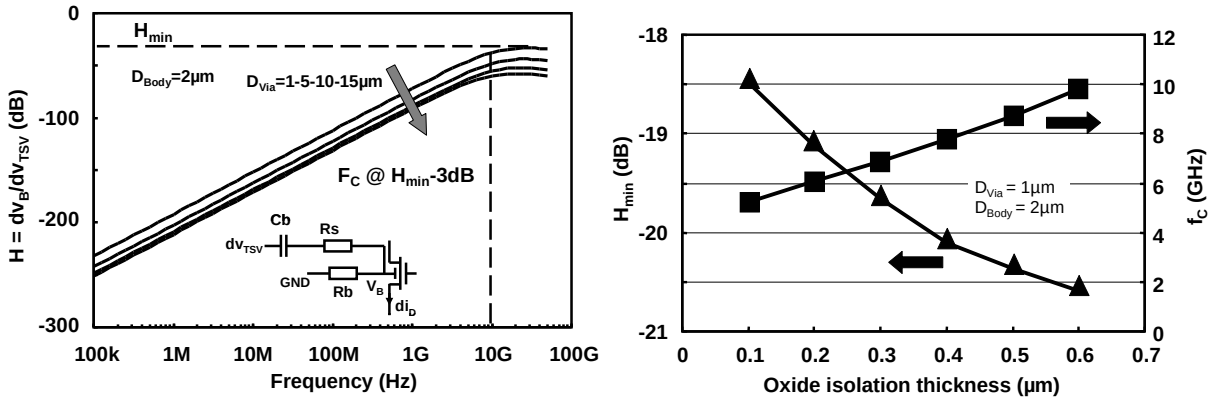

Figure 6. (Left) Transfer function dV_B / dV_{TSV} versus frequency and (Right) figures-of-merit versus oxide isolation thickness.

For low frequency applications, the electrostatic coupling between the TSV and the body is pretty weak. It becomes significant for frequencies higher than 100 MHz. Increasing the distance between TSV and body contact affects the coupling at high frequency but can be insufficient for a low noise amplifier.

For better isolation, an obvious solution is to increase the barrier oxide thickness during the process. However, as illustrated on Figure 6 (Right), this technological parameter has a low impact on H_{min}. Only the cut-off frequency f_C is affected by the barrier oxide thickness. This solution is not efficient for robust design.

For analog applications, the impact of the TSV depends on the frequency operation and the noise figure needs. For example, in the case of high-gain amplifier, the TSV could inject noise into amplifier chain. A solution consists in guarding the TSV using another TSV connected to the ground. This solution will be probably more efficient than a guard ring using body contact (less deep). Nevertheless, for general case in analog applications, the impact of TSV must be annihilated by using a guard ring.

3D upgrade of design environment using standard tools

As there is no commercial 3D-suitable design environment yet, designing 3D test circuitries first appears hazardous. Very few research teams are working to achieve a 3D standard-cell place and route tool and a 3D circuit layout editor [7,11]. The primary goal consists in upgrading the 65 nm advanced technology design kit to allow simple 3D sensitive cells design. Place & Route automation is not allowed here. This procedure works only for simple logic circuits on two active strata, with few gates that should be placed and routed by hand. To achieve 3D design upgrade, the new design rules previously defined are included in the 65nm CMOS technology DRM and a new layout methodology is implemented. This work is carried out with Cadence design environment. The proposed approach is depicted on Figure 7.

The layout sequence can be split up in four steps:

1. Layout generation of bottom tier: create the whole bottom layout with TSV layers.
2. "Mirror view" generation of bottom tier layout: allow to flip the bottom tier layout and create a mirror view of the TSV passing through top stratum.
3. Layout generation of flipped top tier: create the top tier layout by taking into account the TSV locations coming from the bottom tier according to the bottom layout mirror view.
4. Final layout generation: allow to layout the top metal interconnections between TSV and I/O.

Simple logic circuits designed for test can be achieved using this layout methodology with Cadence design environment.

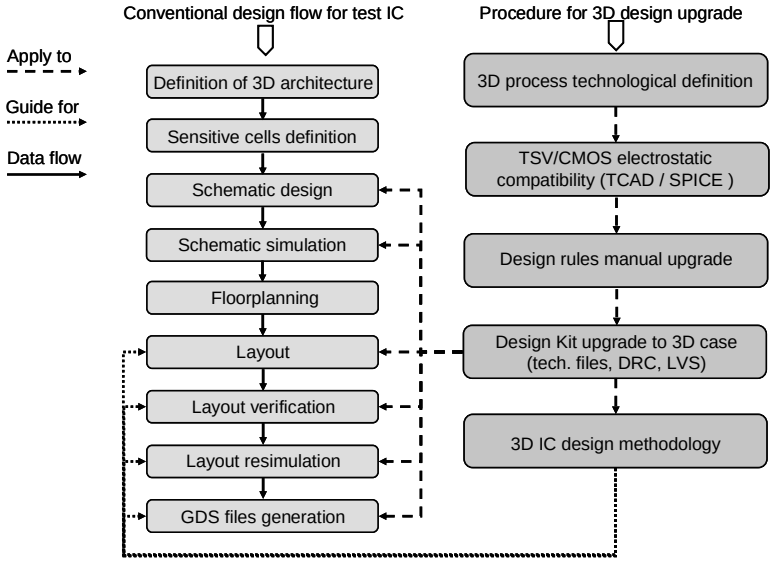

Figure 7. Customized design flow for 3D IC testability

Conclusion

3D integration is considered as a breakthrough technology with a promising potential. Moreover, 3D integration can be adapted to a large field of applications. Up to now, TSV technology development and 3D IC design are the two main challenges of 3D integration. We showed that TSV have a certain electrostatic impact on advanced technology devices. From this statement, parasitic effects could be decreased if TSV-CMOS spatial configurations are optimized. A SPICE-based model calibrated on a FEM-based numerical model has been developed. This easy-to-use model allowed to estimate TSV impact on circuit performances both in analog and digital applications. As a result, no specific design rules are necessary for digital operating mode. Nevertheless, TSV operation involves parasitic coupling for frequencies higher than 100 MHz in analog mode. In this case, specific design rules have been defined in order to ensure a reliable electrical compatibility. These new design rules defined both from the coupling study and technological requirements allowed to update the 65 nm technology design kit. A 3D-dedicated layout methodology has been implemented. Even if our design flow is place-and-route limited, it allows manufacturing of 3D sensitive cells for test. From now on, a real in-depth revision of current design environments will ensure 3D-based architectures to become a relief to interconnect-driven IC design [1,2,11].

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